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*Choi, L.; Pen-Chung Yew;*

Supercomputing '94. Proceedings, 14-18 Nov 1994

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**2 A software engineering methodology to optimize caching in multi-processor DSP architectures: TMS320C80 results towards the real-time execution of low level image processing**

*Lohier, F.; Garda, P.;*

Application-Specific Systems and Software Engineering and Technology, 1999. ASSET '99. Proceedings. 1999 IEEE Symposium on

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*Doallo, R.; Fraguela, B.B.; Zapata, E.L.;*

Parallel and Distributed Processing, 1999. PDP '99. Proceedings of the Seventh Euromicro Workshop on , 3-5 Feb 1999

Page(s): 331 -338

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#### 2 Performance modelling and evaluation for the XMP shared-bus multiprocessor architecture

*Chiung-San Lee; Tai-Ming Parng; Jew-Chin Lee; Cheng-Nan Tsai; Kwo-Jean Farn;*

Parallel and Distributed Systems, 1994. International Conference on , 19-22 Dec 1994

Page(s): 446 -453

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#### 3 A fast low power embedded cache memory design

*Zhao Xue-mei; Ye Yi-zheng; Yu Ming-yan; Li Xiao-ming;*

ASIC, 2001. Proceedings. 4th International Conference on , 2001

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#### 4 Modeling live and dead lines in cache memory systems

*Mendelson, A.; Thiebaut, D.; Pradhan, D.K.;*

Computers, IEEE Transactions on , Volume: 42 Issue: 1 , Jan 1993

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